QSFP-4SFP10G-AOC-xxM

40G QSFP+ To 4x10G SFP+ Breakout Active Optical Cable

FEATURES

- 4 channels full-duplex transceiver modules
- Transmission data rate up to 10Gbps per channel
- 4 channels 850nm VCSEL array
- 4 channels PIN photo detector array
- Internal CDR circuits on both receiver and transmitter channels
- Support CDR bypass
- Low power consumption <2.5W
- Hot Pluggable QSFP form factor

- Maximum link length of 300m on OM3 Multimode Fiber (MMF)and 400m on OM4 MMF
- Single MPO connector receptacle
- Built-in digital diagnostic functions
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant(lead free)

Applications

- IEEE 802.3ba 40GBASE-SR4
- IEEE 802.3be 10GBASE-SR
- InfiniBand SDR/DDR/QDR
- High-Performance Computing (HPC) clusters
- Servers, switches, storage and host card adapter

Description

Fibersum’ s 40G QSFP+ to 4x 10G SFP+ breakout Active Optical Cables (AOCs) offer IT professionals a cost-effective interconnect solution for merging 40G QSFP+ and 10G SFP+ enabled host adapters, switches and servers. For typical applications, users can install this breakout or splitter cable between an available QSFP+ port on 40GE switch and feed up to 4 upstream SFP+ enabled 10GE switches. Each cable features a single SFF-8436 compliant QSFP+ connector rated for 41.2Gb/s on one end and 4 SFF-8431 complicant SFP+ connectors rated for 10.3Gb/s each

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Supply Temperature	VCC	-0.3	3.6	V	
Input Voltage	VIN	-0.3	VCC+0.3	V	
Storage Temperature	Tst	-20	85	degC	1
Case Operating	Top	0	70	degC	
Humidity(non-condensing)	Rh	5	95	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	+85	degC	
Relative Humidity (non-condensation)	RS	-	85	%	
Operating Case Temperature	Topc	0	+70	degC	1
Supply Voltage	VCC3	3.14	3.47	V	
Data Rate Per Lane		1	25.78	Gb/s	

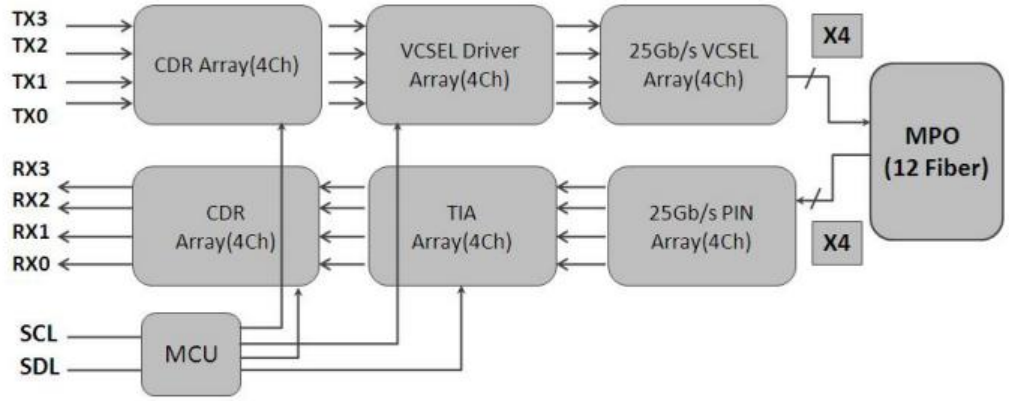


Figure1. Module Block Diagram

40GBASE-SR4 QSFP+ is one kind of parallel transceiver. VCSEL and PIN array package is key technique, through I2C system can contact with module

Paramete	Symb	Min	Typical	Ma	Unit
Differential input impedance	Zin	90	1	110	ohm
Differential Output impedance	Zout	90	1	110	ohm
Differential input voltage amplitude	ΔVin	300		1100	mVp-p
Differential output voltage amplitude	ΔVout	500		80	mVp-p
Ske	Sw			30	ps
Bit Error Rate	BR			E-	
Input Logic Level High	VIH	2.0		VC	V
Input Logic Level Low	VIL	0		0.	V
Output Logic Level High	VOH	VCC-0.5		VC	V
Output Logic Level Low	VOL	0		0.	V

Note :

1. BER=10^-12; PRBS 2^31-1@10.3110Gbps.
2. Differential input voltage amplitude is measured between TxnP and TxnN
3. Differential output voltage amplitude is measured between RxNP and RxnN

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Centre Wavelength	λc	840	850	860	nm	-
RMS spectral width	Δλ	-	-	0.65	nm	-
Average launch power, each lane	Pout	-7.5	-	2.5	dBm	-
Difference in launch power between any two lanes				4	dB	-
Extinction Ratio	ER	3	-	-	dB	-
Peak power, each lane				4	dBm	-
ransmitter and dispersion penalty (TDP),	TDP			3.5	dB	-
Average launch power of OFF transmitter, each lane				-30	dB	-
Eye Mask coordinates: X1, X2, X3, Y1, Y2, Y3	SPECIFICATION VALUES 0.23, 0.34, 0.43, 0.27, 0.35, 0.4					Hit Ratio = 5x10-5
Receiver						
Centre Wavelength	λc	840	850	860	nm	-
Stressed receiver sensitivity in OMA, each lane				-5.4	dBm	1
Maximum Average power at receiver input, each lane				2.4	dBm	-
Receiver Reflectance				-12	dB	-
Peak power, each lane				4	dBm	-
LOS Assert		-30			dBm	-
LOS De-Assert – OMA				-7.5	dBm	-
LOS Hysteresis		0.5			dB	-

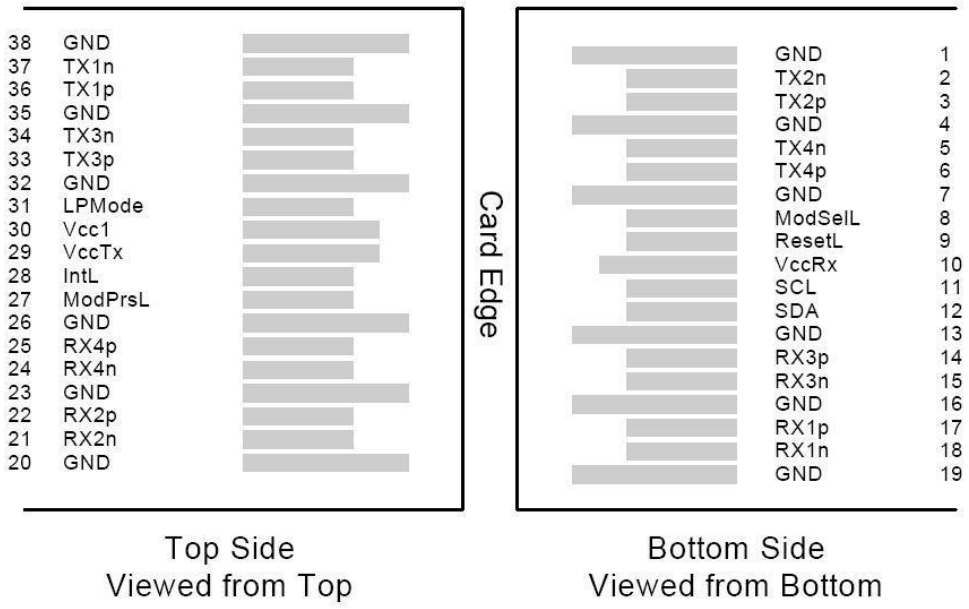
Note :

1 · Measured with conformance test signal at TP3 for BER = 10e-12

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module	1
2	CML-I	Tx2-	Transmitter inverted data input	
3	CML-I	Tx2+	Transmitter non-inverted data input	
4		GND	Module	1
5	CML-I	Tx4-	Transmitter inverted data input	
6	CML-I	Tx4+	Transmitter non-inverted data input	
7		GND	Module	1
8	LVTTL-I	MODSEIL	Module Select	2
9	LVTTL-I	ResetL	Module Reset	2
10		VCCRx	+3.3v Receiver Power Supply	
11	LVCMOS-I	SCL	2-wire Serial interface clock	2
12	LVCMOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module	1
14	CML-O	RX3+	Receiver non-inverted data output	
15	CML-O	RX3-	Receiver inverted data output	
16		GND	Module	1
17	CML-O	RX1+	Receiver non-inverted data output	
18	CML-O	RX1-	Receiver inverted data output	
19		GND	Module	1
20		GND	Module	1
21	CML-O	RX2-	Receiver inverted data output	
22	CML-O	RX2+	Receiver non-inverted data output	
23		GND	Module	1
24	CML-O	RX4-	Receiver inverted data output	
25	CML-O	RX4+	Receiver non-inverted data output	
26		GND	Module	1
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND	
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Module	1
33	CML-I	Tx3+	Transmitter non-inverted data input	
34	CML-I	Tx3-	Transmitter inverted data input	
35		GND	Module	1
36	CML-I	Tx1+	Transmitter non-inverted data input	
37	CML-I	Tx1-	Transmitter inverted data input	
38		GND	Module	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10k ohms on host board to a voltage between 3.15Vand 3.6V.



ModSelL Pin

Figure2. Electrical Pin-out Details

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Fibersum QSFP AOC operate in the low power mode (less than 1.5 W power consumption) This pin active high will decrease power consumption to less than 1w

ModPrsL Pin

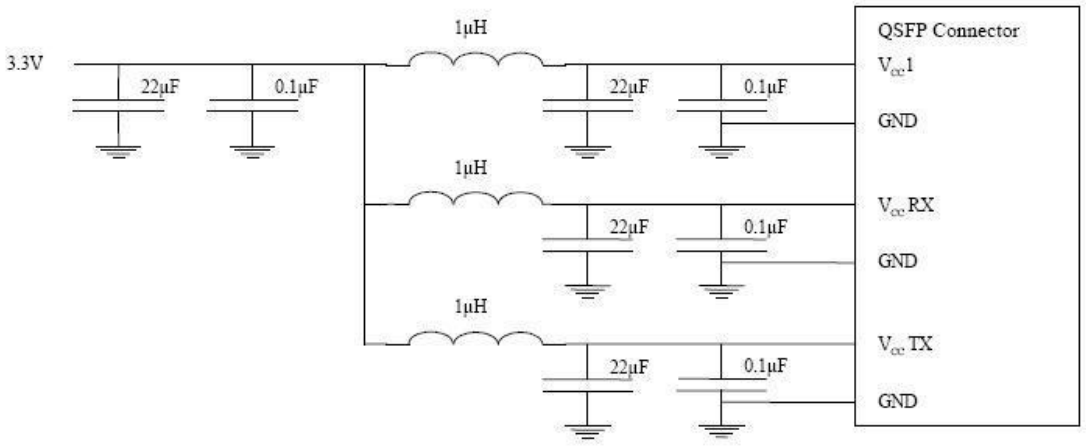
ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure3.



Host Board Power Supply Filtering

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics monitoring function is available on all Fibersum QSFP AOCs. A 2-wire serial interface provides user to contact with module.

The structure of the memory is shown in Figure 4. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function.

The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag

Timing for Soft Control and Status Functions

Parameter	Symbol	Max	Unit	Conditions
Initialization Time	t_init	2000	ms	Time from power on[1], hot plug or rising edge of Reset until the module is fully functional[2]
Reset Init Assert Time	t_reset_init	2	μs	A Reset is generated by a low level longer than the minimum reset pulse time present on the
Serial Bus Hardware Ready Time	t_serial	2000	ms	Time from power on[1] until module responds to data transmission over the 2-wire serial
Monitor Data Ready Time	t_data	2000	ms	Time from power on[1] to data not ready, bit 0 of
Reset Assert Time	t_reset	2000	ms	Time from rising edge on the ResetL pin until the module is fully functional[2]
LPMode Assert Time	ton_LPMode	100	μs	Time from assertion of LPMode (Vin:LPMode = Vih) until module power consumption enters lower Power Level
IntL Assert Time	ton_IntL	200	ms	Time from occurrence of condition triggering IntL
IntL Deassert Time	toff_IntL	500	μs	Time from clear on read[3] operation of associated flag until Vout:IntL = Voh. This includes deassert
Rx LOS Assert Time	ton_los	100	ms	Time from Rx LOS state to Rx LOS bit set and IntL asserted
Tx Fault Assert Time	ton_Txfault	200	ms	Time from Tx Fault state to Tx Fault bit set and IntL asserted

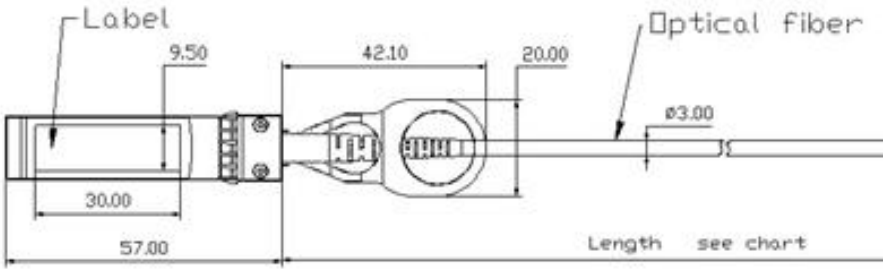
Flag Assert Time	ton_flag	200	ms	Time from occurrence of condition triggering flag to associated flag bit set and IntL asserted
Mask Assert Time	ton_mask	100	ms	Time from mask bit set[4] until associated IntL assertion is inhibited
Mask Deassert Time	toff_mask	100	ms	Time from mask bit cleared[4] until associated IntlL operation resumes
ModSelL Assert Time	ton_ModSelL	100	μ s	Time from assertion of ModSelL until module responds to data transmission over the 2-wire
ModSelL Deassert Time	toff_ModSelL	100	μ s	Time from deassertion of ModSelL until the module does not respond to data transmission over the 2-wire serial bus
Power_over-ride or Power-set Assert Time	ton_Pdown	100	ms	Time from P_Down bit set [4] until module power consumption enters lower Power Level
Power_over-ride or Power-set Deassert Time	toff_Pdown	300	ms	Time from P_Down bit cleared[4] until the module is fully functional3

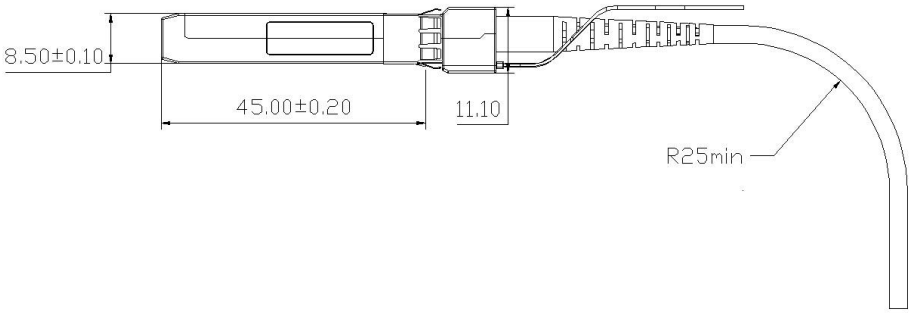
Note :

1. Power on is defined as the instant when supply voltages reach and remain at or above the minimum specified value.
2. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 deasserted.
3. Measured from falling clock edge after stop bit of read transaction.
4. Measured from falling clock edge after stop bit of write transaction.

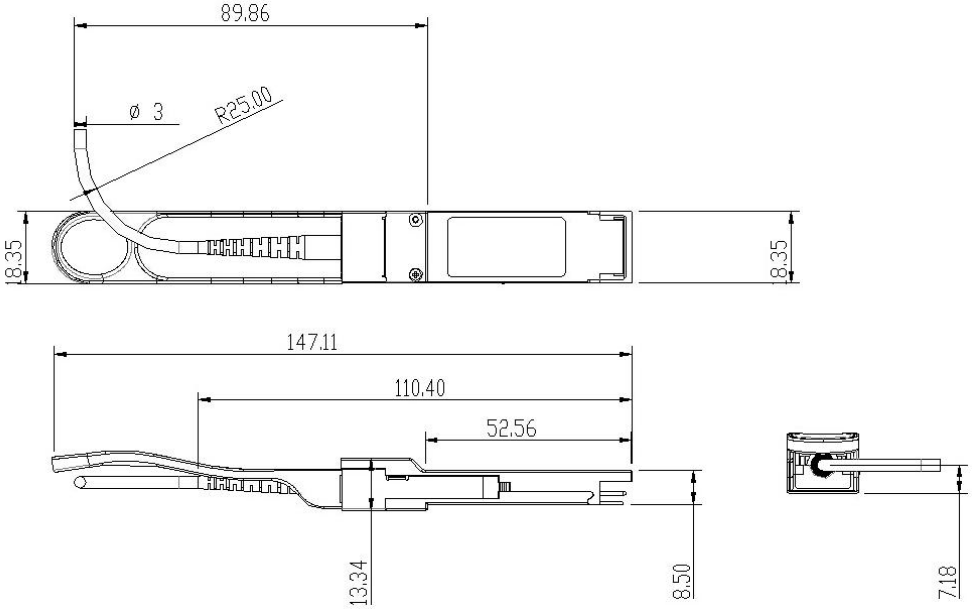
Mechanical Dimensions

SFP+ AOC end Mechanical Specifications





QSFP+ AOC end Mechanical Specifications



ESD

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007)

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